APPENDIX 3

Back gated CMOS on SOIAS For Dynamic Threshold Voltage Control

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Abstract

Simultaneous reduction of supply and threshold voltages for low power design without suffering performance losses will eventually reach the limit of diminishing returns as static power dissipation becomes a significant portion of the total power equation. In order to meet the opposing requirements of high performance and low power, a dynamic threshold voltage control scheme is needed. A novel SOI technology was developed whereby a back-gate was used to control the threshold voltage of the front-gate; this concept was demonstrated on a selectively scaled CMOS process.

Introduction

There have been numerous studies on the merits of fully depleted (FD) SOI CMOS and its implications for low power electronics. Various researchers have exploited the use of FD SOI in dual-gated devices in which the top and bottom gates are tied together, resulting in enhanced transconductance [1, 2, 3, 4]. More recently, another group had demonstrated the concept of dynamic threshold voltage control by tying the body to the gate [5]. We have developed a technology, silicon-on-insulator-with-active-substrate (SOIAS), to fabricate back gated FD CMOS devices by capitalizing on existing SIMOX, wafer bonding, and thinning technologies. The back-gate controls the threshold voltage (V_t) of the front-gate device since the surface potentials at the front and back interfaces are coupled in FD SOI devices. The NMOS and PMOS back-gates are switched independently from each other and the front-gate. This paper describes the development of the SOIAS technology, and an evaluation for low-power logic applications.

SOIAS Preparation and Device Fabrication

The SOIAS substrate is a multilayered blanket film stack consisting of the silicon wafer, oxide, intrinsic polysilicon, back-gate oxide, and silicon film. These substrates were prepared using either bonded SIMOX or etched-back bulk wafers. For the bonded SIMOX process, the back gate oxide to be was formed by dry oxidation and intrinsic amorphous silicon was deposited as the

back-gate to be material. The handle wafer had an oxide/nitride stack. The SIMOX wafer was then bonded to the handle wafer, and annealed in N_2 at 1000 °C for one hour. The bonded wafers were then etched in 25% TMAH to remove the bulk of the SIMOX wafer, stopping on the buried oxide. Nitride was used on the handle wafer because it has a higher selectivity against silicon in TMAH than oxide and the entire thickness of the wafer had to be etched away. The bulk bonding and etch back process is similar to the SIMOX process except the device wafer was thinned down by chemical/mechanical polishing to a thickness of approximately 0.5 μm. Localized plasma thinning [6] was then used to reduce the thickness to approximately 0.2 μm. Final thinning of the silicon film was accomplished with thermal oxidation and wet oxide strip. Fig. 1 depicts the SOIAS preparation for both processes.
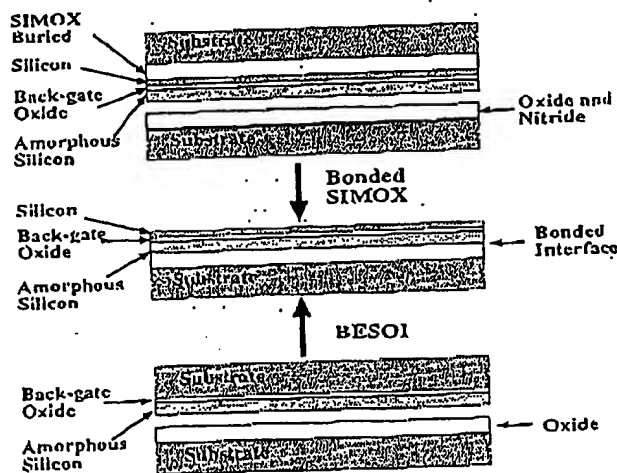

Figure 1: SOIAS preparation using bonded SIMOX and BE-SOI processes.

The back-gates were formed by ion implantation through the silicon film in two masking steps, resulting in islands of p+ and n+ polysilicon insulated by intrinsic poly. The silicon film was also doped to set the zero back-gate bias value for the front-gate V_t. Using the same type of doping in the back-gate poly and silicon film re-

sulted in near-zero flatband voltage at the back-gate. The front-gate device is then built as in a conventional SOI CMOS process using LOCOS isolation. Fig.2 illustrates the final device schematic. Fig.3 shows the effective electron mobility versus effective transverse electric field of the front-gate device for conventional SIMOX and SOIAS. The universality of the curves indicates no apparent difference between the SOIAS and SIMOX substrates from a device operation point of view. The coupling between the front and back-gates depends on the ratio of the critical film thicknesses: front-gate oxide thickness (t_{fox}), silicon film thickness (t_{si}), and back-gate oxide thickness (t_{box}). We have demonstrated SOIAS with 9 nm t_{fox}, 40 nm t_{si}, and 100 nm t_{box} nominal design parameters in a selectively scaled 1 μm baseline CMOS technology.
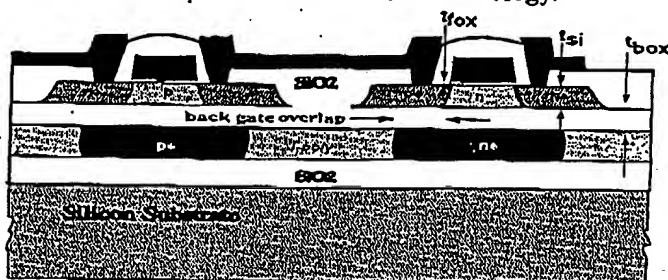
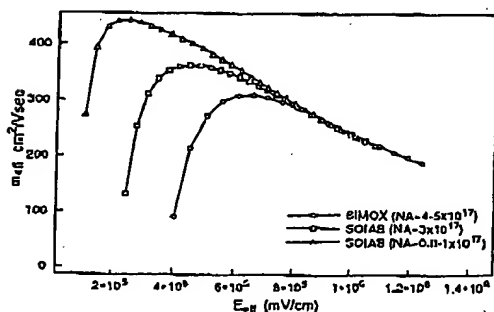Figure 2: SOIAS back-gated CMOS device schematic.

Figure 3: Effective electron mobility for SIMOX and SOIAS.

Device Results

Figures 4-7 show the I-V and subthreshold device characteristics for NMOS and PMOS at two different threshold voltages tuned by biasing the back-gate. A 250 mV change in threshold voltage results in a 3.5-4 decade reduction in off current and a 50-80% current increase at 1 V operation for PMOS and NMOS respectively.

Fig. 8 shows the maximum and minimum tunable V_t limits for the above nominal design parameters. The x-axis is nominal designed V_t which is the threshold voltage at zero back-gate bias. The y-axis, tunable V_t, is obtained by applying various back-gate biases. The tunable V_t
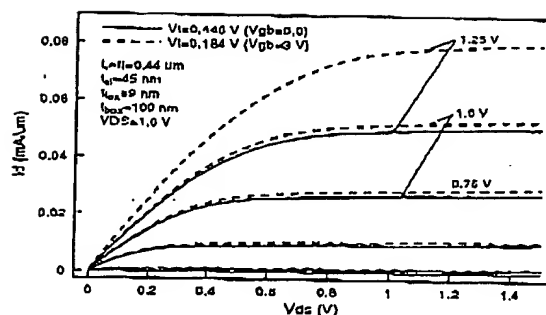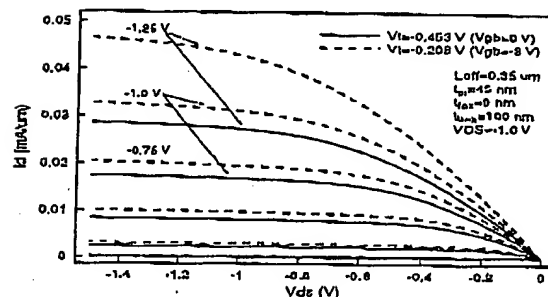
Figure 4: NMOS I-V tuned at different V_t's.

Figure 5: PMOS I-V tuned at different V_t's.

range is quite large for fully depleted back interface, as can be seen for the lowest V_t case at zero back-gate bias. Even for the partially depleted highest V_t case, there is still a reasonable tuning range. This has implications for making FD SOI a viable technology since the threshold voltage and the device operating mode can be controlled precisely by the back-gate. As may be seen in Fig. 8, V_t may be fine tuned over a wide range despite variations in t_{si}(average thickness=48.4 nm, maximum thickness= 69.9 nm and minimum thickness=37.6 nm) and L_{eff}. For example, a nominal V_t of 500 mV may be reached even for a $\pm$ 400 mV deviation by using a $\pm$5-6 V back-gate bias. Fig. 9 shows a 101-stage ring oscillator frequency as a function of varying the back-gate-controlled V_t for either the NMOS or PMOS. In Fig.10, both the NMOS and PMOS V_ts were switched low to achieve a 36% increase in speed.

Application to Low Power Systems

We have chosen to assume a model of operation in which "functional units," or modules, share a common V_t. Under this model, an active system's idle components are left in a low-leakage state. In the modeling of a hypothetical microprocessor's energy dissipation, the modules under consideration are the ALU adder unit, the shifter, and the integer multiplier. We have developed total energy equations including switching and static energies for
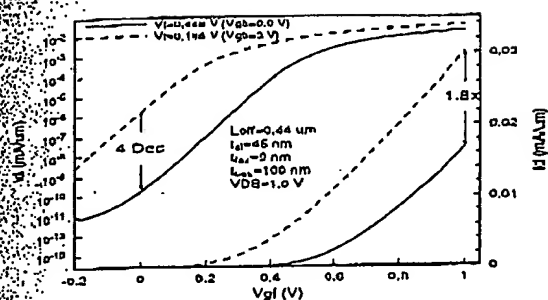
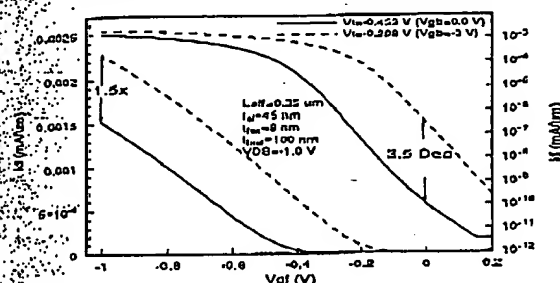BEST AVAILABLE COPY

Figure 6: NMOS subthreshold characteristics.

Figure 7: PMOS subthreshold characteristics.

SOIAS and a benchmark optimized SOI technology in order to analyze the applicability of the SOIAS technology to low power static CMOS logic.

$$E_{SOIAS} = ma(\gamma C_1 V_{dd}^2 + I_{off(low)} V_{dd} t_{cyc})$$
$$+ (1 - ma) I_{off(high)} V_{dd} t_{cyc} + bga C_{box} V_b^2$$
$$E_{SOI} = ma(\gamma C_2 V_{dd}^2) + I_{off(low)} V_{dd} t_{cyc}$$

These equations include:
(a) *Algorithm and architecture parameters:*
ma = module activity factor
bga = back-gate activity factor

Figure 8: Tunable V_t ranges by back-gate biasing.

γ = node switching probability during active period
(b) *Technology and architecture parameter:*
$t_{cycle} = 1/f_{clock}$
(c) *Technology parameters:*
$C_{1,2}$ = total switching capacitance (gate capacitance + front-gate overlap capacitance + fringing capacitance + back-gate overlap capacitance)
$I_{off(low)}$ = low V_t off current
$I_{off(high)}$ = high V_t off current
C_{box} = back-gate oxide capacitance
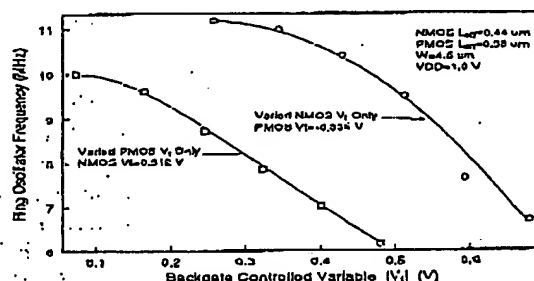V_b = back-gate bias

Figure 9: 101 stage ring oscillator output frequency as varied by changing V_t.

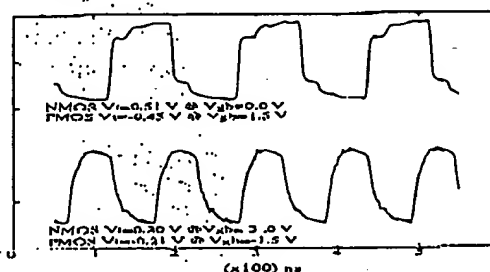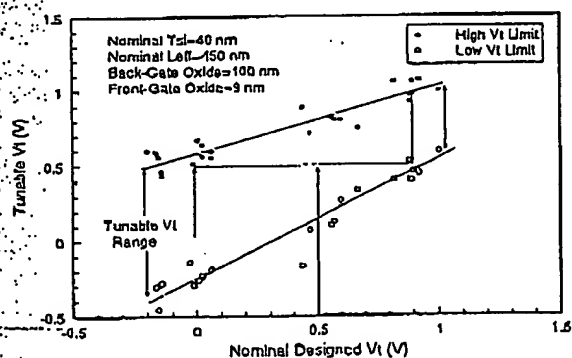

Figure 10: Ring oscillator output at different V_t's tuned by back-gate bias.

The simulation parameters are: t_{si}=40 nm for the practical limit of thinning the silicon film, t_{fox}=7 nm for a 0.25 μm L_{eff} technology; γ, the probability of gate switching in one active cycle is 40% (γ in general is a strong function of bit transition probabilities), 100 MHz clock frequency, and $V_{dd} = 1.0$ V. The circuit operates by switching the back-gate and lowering V_t when a module is active, and raising the V_t when the module is inactive, satisfying the opposing requirements of high performance and low standby leakage at low power supply voltages. The applicability of SOIAS technology is a function of transistor and functional block usage. To determine functional block usage patterns (ma and bga), we performed a series of program profiling experiments using the ATOM code [7] instrumentation interface for a particular microprocessor implementation, compiler technology, and various

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algorithms.

The ratio of the total energy dissipation for SOIAS and SOI was analyzed as a function of algorithm and architecture dependent parameters(ma and bga, see Fig.11), as well as technology dependent parameters(t_{box} and source/drain overlap with back gate, Fig.12. The SOIAS technology is most suitable for systems which operate in burst mode, as shown in Fig.11. Near continuous functional block usage which does not exhibit strong temporal locality (e.g adder and shifter in a continuously computing system) does not favor the SOIAS technology. In a system which is frequently idle while awaiting I/O, such an X server which is active 2% of the time, the SOIAS technology dissipates less energy than conventional SOI: 43% for the adder (ma=69.7%, bga=21.3%), 80% for the shifter(ma=10.9%, bga=8.7%) , and 97% for the multiplier(ma=0.83%, bga=0.83%). For low activity modules (the multiplier and shifter), the design space in favor of the SOIAS technology spans the entire parameter range under study for both t_{box} and overlap/L_g (Fig.12a). For high activity modules (the adder), the design space in favor of SOIAS technology strongly depends on the ma/bga ratio. Note for the adder (Fig.12b), there is an optimal range of t_{box} which allows the most overlap where the energy is minimized. Therefore, when the ma and bga values are high, their ratio determines the range of optimal back-gate oxide thicknesses with the maximum design latitude in the back-gate overlap in the technology design space.

Figure 12: Energy ratio of SOI and SOIAS in the technology design space for functional modules with various activity factors.
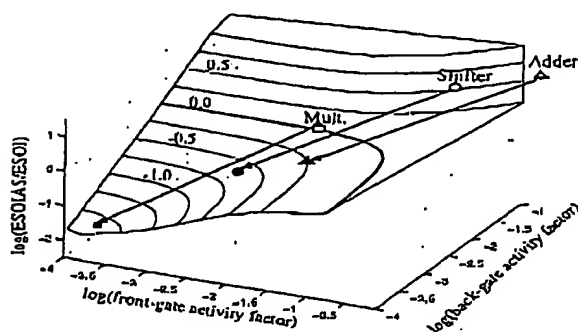
burst mode.

Figure 11: Energy ratio of SOI and SOIAS technologies for systems that are frequently in use (open symbols) and those that are mostly idle (2% usage for X server)(filled symbols).

Conclusions

Dynamic control of threshold voltage has been demonstrated in the novel SOIAS technology developed through bonded SIMOX and BESOI processes. Furthermore, the flexibility in threshold voltage control through back-gate biasing from partially depleted to fully depleted devices provides a viable option for FD SOI. Finally, the applicability of the SOIAS technology for low power design was found to be most suitable for systems which operate in
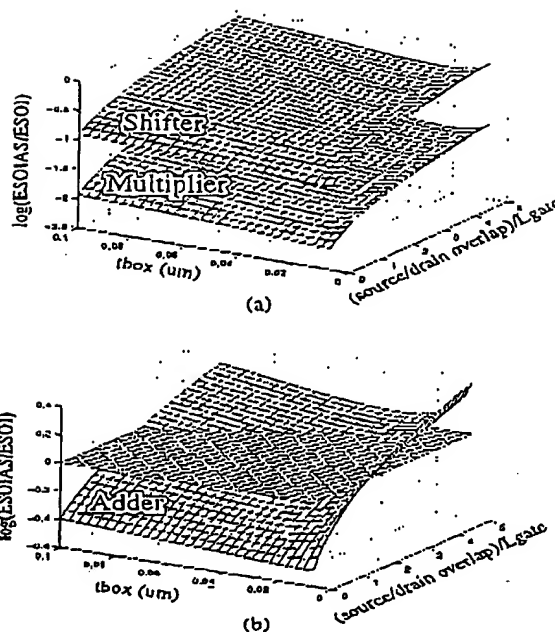
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